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INTRODUCTION

ADS brings to you advanced capabilities formerly unavailable to micro-computers. Markets such as business accounting, word processing, scientific programming, medical analysis, communications switching, process control, etc., will find the ADS 6809 S-100 single board computer to be the optimum choice.

BOARD CONSTRUCTION

1) Install the sockets, noting the orientation of the sockets on the board's silk-screened parts layout and solder them in place.

2) While observing orientation of the polarized capacitors on the silk-screened parts layout, install the capacitors and solder in place.

3) Solder the resistors in the locations specified on the silk-screen.

4) Place a piece of tape on the board covering the location of the 4MHZ crystal. This insures that the crystal case will not contact traces underneath it. Now solder the MPU crystal and the baud rate generator crystal in their respective locations.

5) Solder the DIP switch in place.

6) Using a 6-32 x 3/8" screw and nut, install the -12V regulator. No heat sink is required because of the minimal current drawn.

7) Again using 6-32 x 3/8" screws and nuts, install the +12V and -5V regulators and their Thermalloy 6073B heatsinks. Use heat sink compound sparingly.

8) Again using 6-32 x 3/8" screws and nuts, install the +5V regulator and its Thermalloy 6061B heatsink. Use heat sink compound sparingly.

9) At this stage, you should refer to section below in order to configure the board to your specifications.

10) With no IC's in place, apply power to the board and test to see that proper voltages are available to all IC's on the board.

11) Now disconnect the power to the board and install the IC's, noting proper pin 1 position (usually denoted by a dot on the pin 1 end).

CONFIGURING THE BOARD

Points at which you are to solder a jumper wire will be referenced by the jumper points' number which can be found on the boards silk-screened parts layout. Refer to Fig. 1 to aid in locating these points. In some cases it may be necessary to solder more than one wire in a jumper hole. For this reason 28 or 30 guage wire is recommended for jumper wires.

I/O ADDRESSING

Input/output occupies 4K bytes of the 64K byte available memory space. The ACIA, PIA and 8080 simulated I/O ports each occupy alK Byte block. I/O addresses may be located on any 4K boundary by connecting jumper #48 to any one of the unused 4K selects, #'s 32-47. (See Table 1). Within this 4K space, the ACIA and the PIA occupy the 2 lower consecutive 1K blocks, respectively, while the 8080 I/O ports occupy the upper 1K block.

NOTE: Since only 256 8080 I/O ports are implemented, the I/O port addresses occur four times within their alloted 1K block. In other words, the values of A8 and A9 are don't cares. The upper 6 bits of the address select that 1K block and only the lower byte of the I/O address determines which particular I/O port is selected. Ex. if jumper #48 connected to #32, then I/O addresses occur ØØØØH-ØFFFH, I/O ports are located ØCØØH-ØFFFH. The following addresses select I/O port #9: ØC09H, ØD09H, ØE09H, ØF09H

X000H	ACIA Status Reg.
X001H	ACIA Data Reg.
	repeats as shown
X400H	PIA A-Data Reg.
	PIA A-Control Reg.
	PIA B-Data Reg.
	PIA B-Control Reg.
	repeats as shown
X800H	not used
XC00H	8080 I/O Port Ø
XC01H	8080 I/O Port 1
XC02H	8080 I/O Port 2
	⋮
XCFFH	8080 I/O Ports 255
	repeats as shown
XFFFH	

X= I/O 4K select

RAM ADDRESSING

RAM occupies up to 2K bytes of the available memory space. It is located on any unused 4K boundary by connecting jumper #49 to any of the unused 4K selects, jumper #'s 32-47 (See Table 1). Within the 4K block, each 1K byte of RAM can be located on any of the four 1K boundaries. This is done by connecting that particular 1K blocks' chip select line, either jumper #26 or #27, to the desired 1K select line, jumper #'s 28-31 (See Table 2).

ROM ADDRESSING

The board provides space for 4 sockets in which ROM, EPROM, or byte wide RAMs can be installed. These sockets can be configured to many different parts' power supplies, chip selects, and address line requirements. Table 3 lists some of the specific parts usable with the board.

CONFIGURING FOR 1K X 8 PARTS.

One of the unused 4K selects, jumper #'s, 32-47 (See Table 1) should be connected to jumper #50. This allots 4K bytes of memory space to the ROM sockets.

The following pairs of jumper #'s should be connected:

4-7)	This configures the decoding
5-8)	for 1K byte parts
18-19)	This connects the 1K byte parts' chip
20-21)	selects to the 1K select lines.
22-23)	
24-25)	

See Table 3 to complete configuration for the specific 1K x 8 parts being used.

CONFIGURING FOR 2K X 8 PARTS.

Two of the 4K selects, jumper #'s 32-47 (See Table 1) should be connected to jumper #'s, 50 and 51. This allots 8K bytes of memory space to the ROM sockets. If you wish to split the 8K bytes into 2 non-contiguous 4K byte blocks, you must connect the lower of the two 4K selects which was used above to jumper #8.

The following pairs of jumper #'s should be connected:

5-7)	This configures the decoding for 2K
)	byte parts.
6-8)	For contiguous 4K blocks
or	
(78 or 79)-8	use the lower 4K select (78 or 79) if noncontiguous 4K blocks

See Table 3 to complete configuration for the specific 2Kx8 parts being used.

CONFIGURING FOR 4K X 8 PARTS.

Since each of these parts occupies 4K bytes, 4 unused 4K selects (jumper #'s 36-47) should be connected directly to the chip selects, jumper #'s 18-24.

See Table 3 to complete configuration for the specific 4Kx8 parts being used.

TABLE I

4K select jumper #'s

#	Address Range
32	0000H - 0FFFH
33	1000H - 1FFFH
34	2000H - 2FFFH
35	3000H - 3FFFH
36	4000H - 4FFFH
37	5000H - 5FFFH
38	6000H - 6FFFH
39	7000H - 7FFFH
40	8000H - 8FFFH
41	9000H - 9FFFH
42	A000H - AFFFH
43	B000H - BFFFH
44	C000H - CFFFH
45	D000H - DFFFH
46	E000H - EFFFH
47	F000H - FFFFH

TABLE II

Ram 1K select jumper #'s

#	Address Range
28	X000H - X3FFH
29	X400H - X7FFH
30	X800H - XBFFH
31	XC00H - XFFFH

Note: X designates 4K RAM select

OTHER JUMPER OPTIONS

MWRITE can be obtained by connecting jumper #61 to #62.

POC* (Power on Clear), (if needed) is obtained by connecting jumper #52 to #55. Note: POC* required for single board operation.

SLAVE CLR* is obtained by connecting jumper #54 to #57 .

RESET* (if needed) is obtained by connecting jumper #53 to #56

pINT*, a control input for interrupts is available by connecting jumper #1 to #2 for a standard interrupt to the processor. Connect #1 to #3 if you desire this signal to generate a fast interrupt request (FIRQ) to the processor. PINT* is already connected to interrupts from the ACIA and can be connected to interrupts from the PIA by connecting jumper #58 and either #59 or #60 for PORT A or PORT B interrupts, respectively.

Baud rate selection is most easily implemented using a DIP switch. CAUTION: Only one baud-rate should be selected at a time.

Default jumper #'s 65 and 66 and upper address line default jumper #'s 67-74 are provided for future memory management.

REFERENCES

For additional information see the following:

Motorola MC6809 data sheet
Motorola MC6821 data sheet
Motorola MC6850 data sheet
Motorola MC6809 Preliminary Programming Manual

S-100 SIGNALS UTILIZED

1 - +8 volts @ 2 amps
2 - +16 volts @ 1/2 amp
3 - XRDY-halts processor when asserted
4 n.c.
5 n.c.
6 n.c.
7 n.c.
8 n.c.
9 n.c.
10 n.c.
11 n.c.
12 - NMI*-non-maskable interrupt
13 n.c.
14 n.c.
15 n.c.
16 n.c.
17 n.c.
18 - SDSB*-disables SMEMF,SINP,SOUT,SHLTA,SWO*,SINTA
19 - CDSB*-disables PHLDA,PSYNC,PDBIN,PWR*,PSTVAL
20 - ground
21 n.c.
22 - ADSB*-disables A0-A15
23 - DODSB*-disables DO0-DO7
24 - Φ-master bus clock
25 - PSTVAL*-address & status valid strobe
26 - PHLDA-indicates processor is halted
27 n.c.
28 n.c.
29 - A5-address bit 5
30 - A4-address bit 4
31 - A3-address bit 3
32 - A15-address bit 15
33 - A12-address bit 12
34 - A9-address bit 9
35 - DO1-data out bit 1
36 - DO0-data out bit 0
37 - A10-address bit 10
38 - DO4-data out bit 4
39 - DO5-data out bit 5
40 - DO6-data out bit 6
41 - DI2-data in bit 2
42 - DI3-data in bit 3
43 - DI7-data in bit 7
44 n.c. (no parallel to SM1 available with MC6809)
45 - SOUT-cycle is '8080' output to device transfer
46 - SINP-cycle is '8080' input from device transfer
47 - SMEMR-cycle is memory read transfer
48 - SHLTA-cycle is halt cycle
49 - CLOCK-2 MHZ 50% utility clock
50 - ground

51 - +8 volts (common with pin 1)
52 - -16 volts @ 1/4 amp
53 - ground
54 - SLAVE CLR*-jumperable to activate with POC*
55 n.c.
56 n.c.
57 n.c.
58 - SXTRQ*-always not asserted
59 n.c.
60 n.c.
61 n.c.
62 n.c.
63 n.c.
64 n.c.
65 n.c.
66 n.c.
67 n.c.
68 - MWRT-memory write=PWR* and not SOUT (jumperable)
69 n.c.
70 - ground
71 n.c.
72 - RDY-sampled on Φ rising edge. Stretches cycles for slow devices. MC6809 stretch limitation is 10 usec.
73 - INT*-interrupt request. Jumperable to MC6809 IRQ or FIRQ
74 - HOLD*-halts processor when asserted
75 - RESET*-jumperable to activate with POC*
76 - PSYNC-indicates start of bus cycle
77 - PWR*-indicates valid data on data out bus. Due to MC6809 limitations data should only be latched on trailing edge.
78 - PDBIN-indicates request for data on data in bus. Data will be latched on trailing edge.
79 - A0-address bit 0
80 - A1-address bit 1
81 - A2-address bit 2
82 - A6-address bit 7
83 - A7-address bit 8
84 - A8-address bit 8
85 - A13-address bit 13
86 - A14-address bit 14
87 - A11-address bit 11
88 - DO2-data out bit 2
89 - DO3-data out bit 7
90 - DO7-data out bit 7
91 - DI4-data in bit 4
92 - DI5-data in bit 5
93 - DI6-data in bit 6
94 - DI1-data in bit 1
95 - DI0-data in bit 0
96 - SINTA-cycle is interrupt or reset vector fetch
97 - SWO*-cycle is write cycle
98 n.c.
99 -- POC*-asserted for 10 msec. at power on(jumperable)
100 - ground

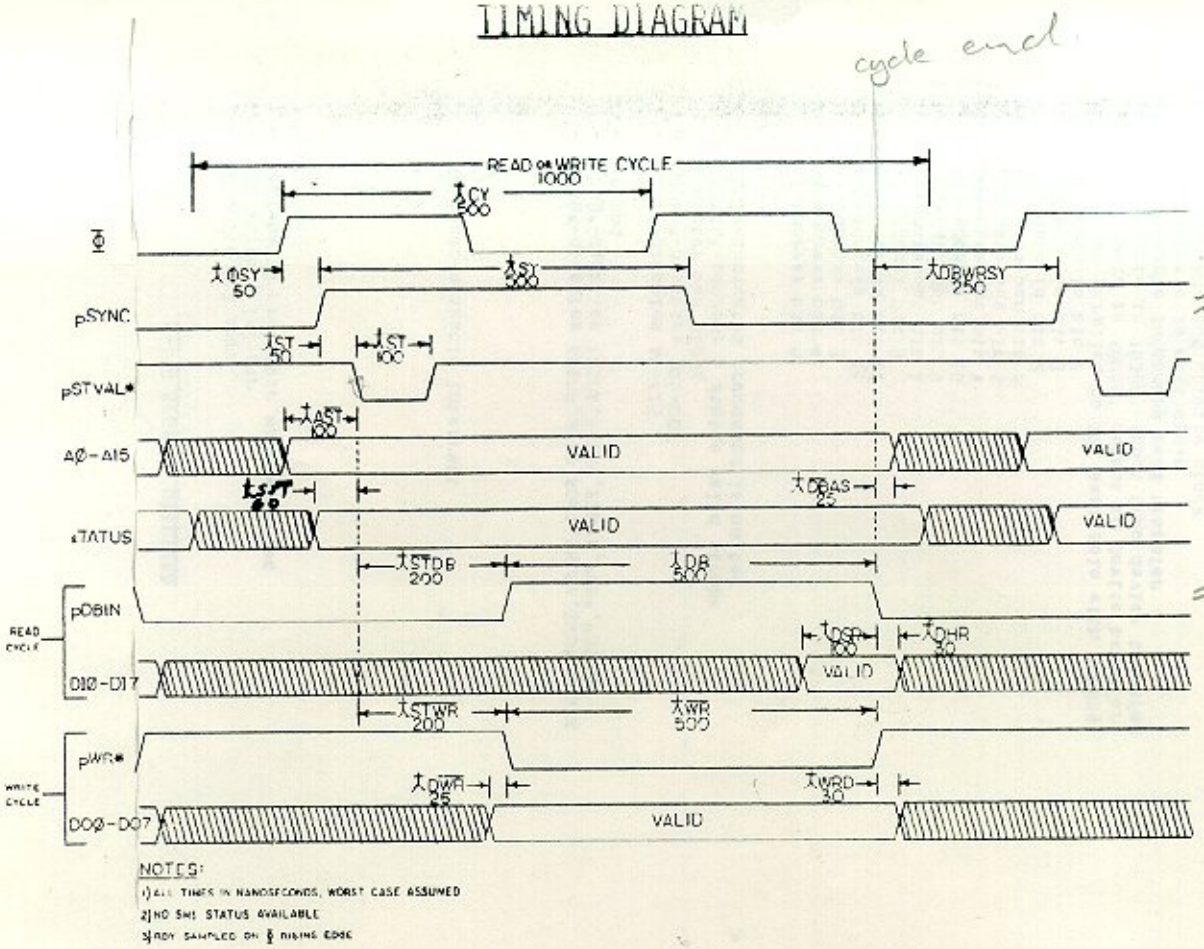
PARTS LIST

6809 SBC

QUANITY	PART	DESCRIPTION	DESIGNATION
2	SN74LS00	:Quad nand gate	U26,27
1	SN74LS02	:Quad nor gate	U29
3	SN74LS04	:Hex inverter	U33,34,36
1	SN74LS05	:Open-collector hex inverter	U35
1	SN74LS08	:Quad nand gate	U25
1	SN74LS10	:Triple nand gate	U28
1	SN74LS14	:Schmitt trigger hex inverter	U32
1	SN74LS74	:Dual D flip-flop	U15
1	SN74LS138	:3 line to 8 line demux	U5
1	SN74154	:4 line to 16 line demux	U16
1	SN74LS155	:Dual 2 line to 4 line demux	U24
8	SN74LS367	:Hex tri-state buffer	U7,8,9,10,11,12,13,14
1	MC1488	:Quad RS-232c driver	U31
1	MC1489	:Quad RS-232c receiver	U30
1	MC6809	:MPU	U6
1	MC6821	:PIA	U19
1	MC6850	:ACIA	U18
1	MC14411	:Baud rate generator	U17
4	2114	:1K x 4 450ns static ram	U20,21,22,23
1	LM323K	:5 V. 3Amp regulator	Q1
1	LM320T-12	:-12 V. 1Amp regulator	Q2
1	LM320T-5	:-5 V. 1Amp regulator	Q4
1	LM340T-12	:12 V. 1Amp regulator	Q3
1	THM6061B	:5 V. regulator heat sink	T1
2	THM6073B	:12 V. & -5 V. heatsinks	T3,4
1	47Pf.	:MPU clock 10 V.	C1
2	470Pf	:Timing	C2,3
7	4.7 Uf	:Tantalum capacitor 25 V.	C4,5,7,8,9,10,11
1	10 Uf	:Tantalum capacitor 16 V.	C6
1	1.0 Uf	:Tantalum capacitor 16 V.	C33
13	0.01 Uf	:Ceramic disc capacitor 25 V.	C's
2	680 ohm	:1/4 watt 5% resistor MPU clock	R1,2
15	1K ohm	:1/4 watt 5% resistor Pull up	R3,4,5,6,7,9,13,14,15 16,18,19,20,21,22
1	~~100~~ 150 ohm	:1/4 watt 5% resistor Timing	R11 + R12
~~1~~	~~220 ohm~~	~~:1/4 watt 5% resistor Timing~~	~~R12~~
1	100K ohm	:1/4 watt 5% resistor Timing	R17
1	1M ohm	:1/4 watt 5% resistor	R23
1	1.843MHz	:Baud rate xtal osc.	X1
1	4.00MHz	:MPU clock xtal	X2
1	10 pin	:Scotch #3446-1002 connector	P1
1	26 pin	:Scotch #3429-1002 connector	P2
1	Switch	:8 Position dip style	S1
13	14 pin	:I/C sockets	
10	16 pin	:I/C sockets	
4	18 pin	:I/C sockets	
7	24 pin	:I/C sockets	
2	40 Pin	:I/C sockets	

Note: R8 and R10 have been omited.

TIMING DIAGRAM



cycle end

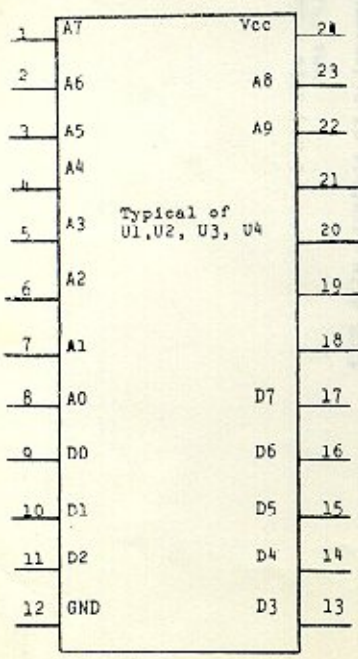
≈ Q . VMA.

Strobe Valid Address?

≈ E.

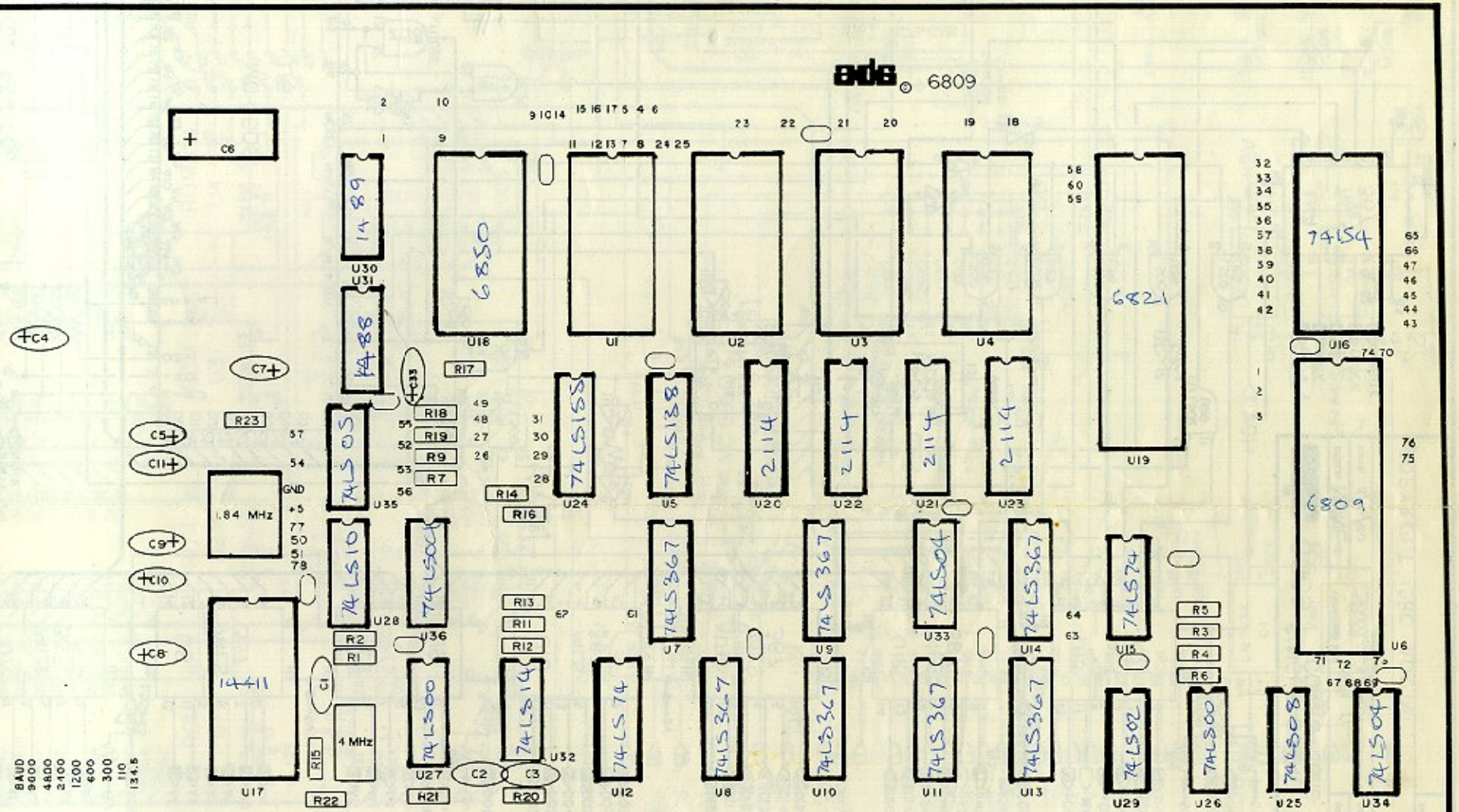
TABLE III

Configuring for some specific memory parts

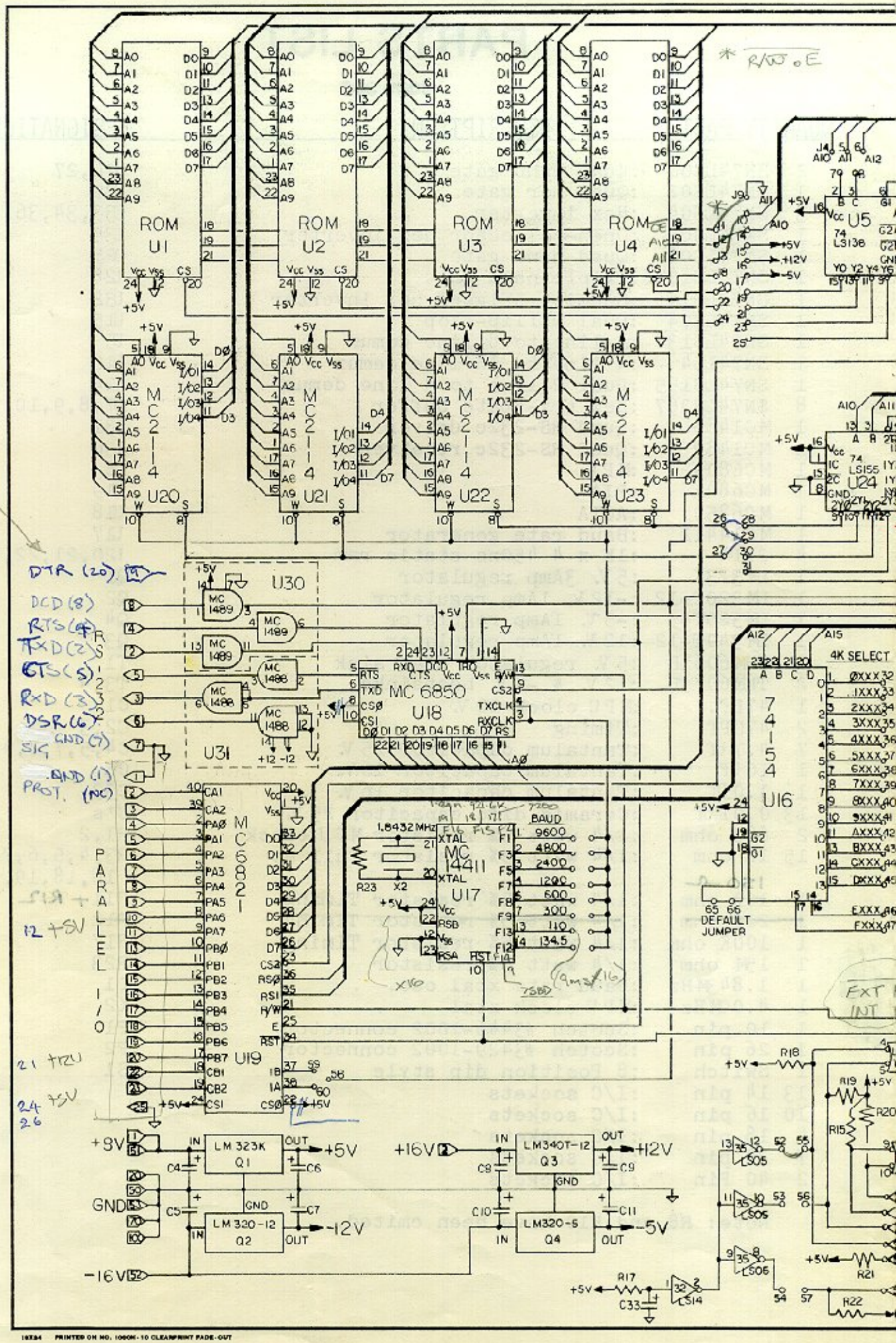


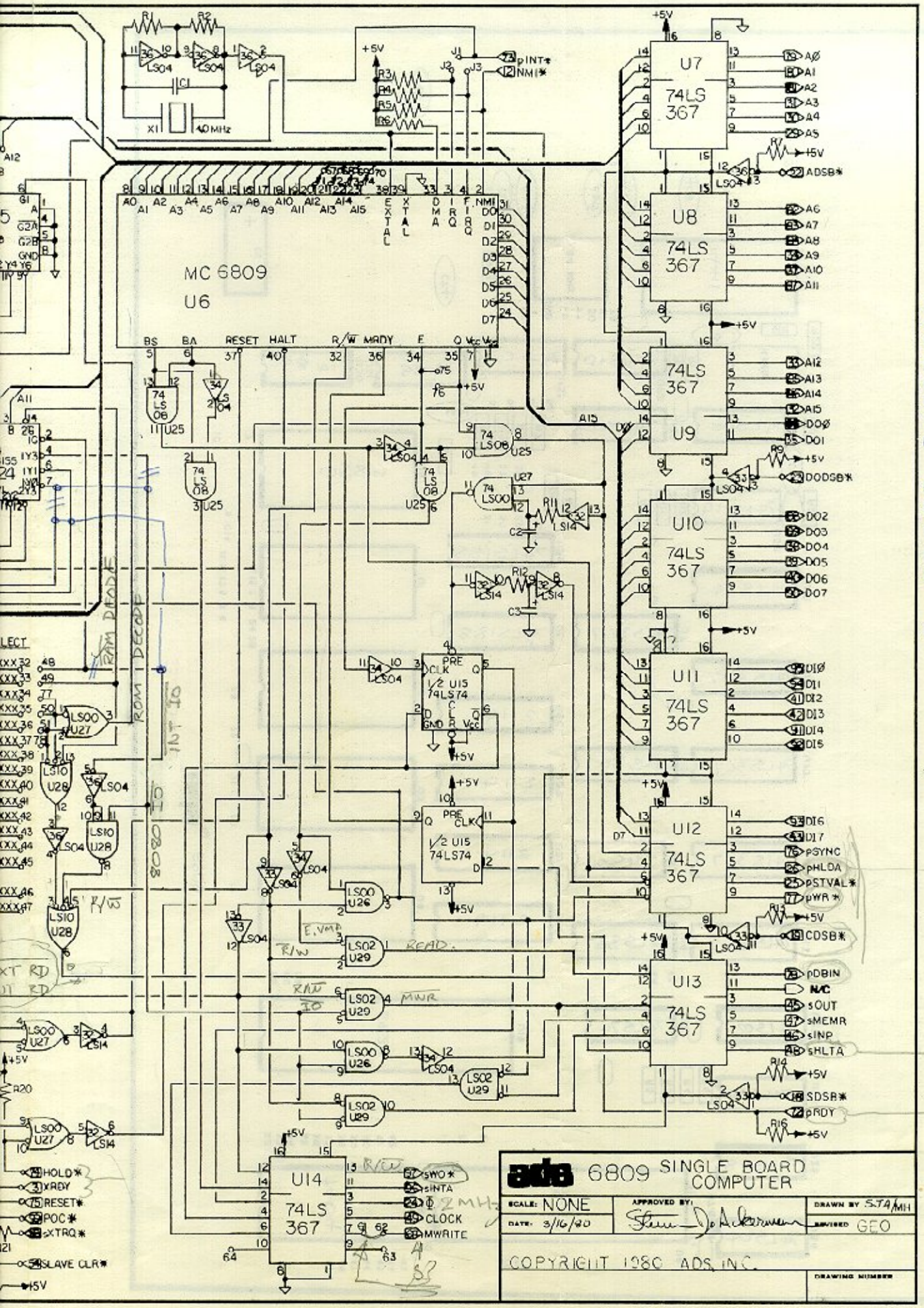
	1KX8				2KX8			4KX8		
	ROM	EPROM	STATIC RAMS		ROM	EPROM	RAM	ROM	EPROMS	
	NEC uPD2308 or INTEL 8308	2708	MK4118 or MK4801	EMM SEMI 8308	NS MM2316E or AMI S4216B	INTEL 2716 or TI TMS2516	OKI M3M 2128-1	NEC uPD2332 or TI TMS4732	TI2532	INTEL 2732
21	-5V J13-J17	-5V J13-J17	$\overline{pWR}$ Note 2	Not Conn.	$\overline{CS}$ Note 3	+5V J13-J15	$\overline{pWR}$ Note 2	$\overline{CS}$ Note 3	+5V J13-J15	A11 J13-J10
20	$\overline{CS}$ Note 4	$\overline{CS}$ Note 1	$\overline{CS}$ Note 1	$\overline{CS}$ Note 1	$\overline{CS}$ Note 4	$\overline{CS}$ Note 1	$\overline{CS}$ Note 1	$\overline{CS}$ Note 4	$\overline{CS}$ Note 1	$\overline{CS}$ Note 1
19	+12V J12-J16	+12V J12-J16	GND J12-J9	Not Conn.	A10 J12-J14	A10 J12-J14	A10 J12-J14	A10 J12-J14	A10 J12-J14	A10 J12-J14
18	$\overline{CS}$ Note 3	GND($\overline{CS}$) J11-J9	GND($\overline{CS}$) J11-J9	$\overline{pWR}$ Note 2	$\overline{CS}$ Note 3	GND($\overline{CS}$) J11-J9	GND($\overline{CS}$) J11-J9	A11 J11-J10	A11 J11-J10	GND($\overline{CE}$) J11-J9

Note 1: See ROM ADDRESSING in manual.
Note 2: $\overline{pWR}$ is obtained by jumpering U26 pin 3 to J13.
Note 3: Mask programmable, connect to +5V or GND as required.
Note 4: Mask programmable, must be active low.



Note 1: There is no R8 or R10.
Note 2: Bypass capacitors are the 13 unmarked ovals.




MC 6809
U6
U7
U8
U9
U10
U11
U12
U13
U14
74LS 367
40 MHz
X1
C1
+5V
ADSB*
DODSB*
CDSB*
SDSB*
pINT*
NMI*
pSYNC
pHLDA
pSTVAL*
pWR*
pDBIN
N/C
sOUT
sMEMR
sINP
sHLTA
pRDY
sWO*
sINTA
Φ 2MHz
CLOCK
MWRITE
HOLD*
XRDY
RESET*
POC*
XTRQ*
SLAVE CLR*
ROM DECODE
I/O DECODE
READ
R/W
E.VMA
MWR
ads
6809 SINGLE BOARD COMPUTER
SCALE: NONE
DATE: 3/16/80
APPROVED BY:
DRAWN BY S.T.A/M.H
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